Ordering number : ENA2255

LE25CB643TT-BH

CMOS IC

64 kb SPI CMOS Serial EEPROM

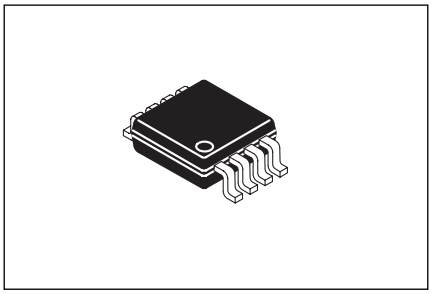
ON Semiconductor®

http://onsemi.com

Overview

The LE25CB643TT-BH (hereinafter referred to as 'this device') is serial peripheral interface EEPROM (Electrically Erasable and Programmable ROM). This device realizes high speed and a high level reliability by incorporating high performance CMOS EEPROM technology. This device is compatible with SPI memory protocol, therefore it is best suited for application that requires re-writable nonvolatile parameter memory. And this device has 32bytes page write function for high speed data re-write.

Function



Micro8

- Capacity : 64k bits (8k × 8 bits)
- Single supply voltage : 2.7V to 5.5V
- Operating temperature : -40ºC to +85ºC
- Interface : SPI Mode0 and Mode3 correspondence
- Operating clock frequency : 5MHz
- Low Power consumption
  - : Standby : 3μA (max.)
  - : Read : 1mA (max.)
  - : Write : 3mA (max.)
- Automatic page write mode : 32 Bytes
- Write cycle time : 5ms
- Erase/Write cycles : 10^6 cycles
- Data Retention : 20 years
- High reliability : Adopts proprietary symmetric memory array configuration (USP6947325) Incorporates a feature to prohibit write operations under low voltage conditions.
- Package : LE25CB643TT-BH Micro8

* This product is licensed from Silicon Storage Technology, Inc. (USA).

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage			-0.5 to +6.5	V
DC input voltage			-0.5 to 5.5	V
Over-shoot voltage			-1.0 to 6.5	V
Storage temperature	Tstg		-65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage			2.7		5.5	V
Operating temperature			-40		+85	°C

DC Electrical Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply current at reading	I_{CCR}	$\overline{CS}$ = 0.1V_{DD}, $\overline{HOLD}$ = $\overline{WP}$ = 0.9V_{DD} SI = 0.1V_{DD}/0.9V_{DD}, SO =open clock frequency = 5MHz, V_{DD} = V_{DD} max			1	mA
Power supply current at writing	I_{CCW}	V_{DD} = V_{DD} max, V_{IN} = 0.1V_{DD}/0.9V_{DD}			3	mA
CMOS standby current	I_{SB}	$\overline{CS}$ = V_{DD}, V_{IN} = V_{DD} or V_{SS} V_{DD} = V_{DD} max			3	μA
Input leakage current	I_{LI}	V_{IN} = V_{SS} to V_{DD}, V_{DD} = V_{DD} max			2	μA
Output leakage current	I_{LO}	V_{IN} = V_{SS} to V_{DD}, V_{DD} = V_{DD} max			2	μA
Input low voltage	V_{IL}	V_{DD} = V_{DD} max	-0.3		0.3V_{DD}	V
Input high voltage	V_{IH}	V_{DD} = V_{DD} min	0.7V_{DD}		V_{DD}+0.3	V
Output low voltage	V_{OL}	I_{OL} = 3.0mA, V_{DD} = 2.7V to 5.5V			0.4	V
Output high voltage	V_{OH}1	I_{OH} = 0.4mA, V_{DD} = 2.7V to 5.5V	0.8V_{DD}			V

Capacitance at Ta = 25°C, f = 1MHz

Parameter	Symbol	Conditions	Ratings	Unit
In/Output pin capacitance	C_{DQ}	V_{DQ} = 0V	12	pF
Input pin capacitance	C_{IN}	V_{IN} = 0V	6	pF

Note: This parameter is sampled and not 100% tested.

AC Electric Characteristics

Input pulse level	$0.2 \times V_{DD}$ to $0.8 \times V_{DD}$
Input pulse rise / fall time	10ns
Output detection voltage	$0.5 \times V_{DD}$
Output load	30pF

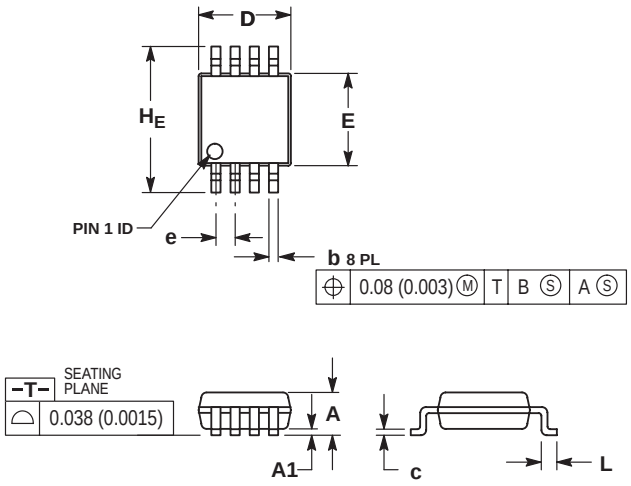
AC characteristic (f_{CLK} = 5MHz Operation) V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Ratings		Unit
		min	max	
Clock frequency	f_{CLK}		5	MHz
SCK High pulse width	t_{CLHI}	90		ns
SCK Low pulse width	t_{CLLO}	90		ns
Input rising, falling time	t_{RF}		1	µs
$\overline{CS}$ Setup time	t_{CSS}	90		ns
SCK Setup time	t_{CLS}	90		ns
Data Setup time	t_{DS}	20		ns
Data Hold time	t_{DH}	30		ns
$\overline{CS}$ Hold time	t_{CSH}	90		ns
SCK Hold time	t_{CLH}	90		ns
$\overline{CS}$ Standby pulse width	t_{CPH}	90		ns
$\overline{CS}$ to High-Z output	t_{CHZ}		150	ns
SCK to output valid	t_V		80	ns
Output data hold time	t_{HO}	0		ns
$\overline{WP}$ Setup time	t_{WPS}	30		ns
$\overline{WP}$ Hold time	t_{WPH}	30		ns
$\overline{HOLD}$ Setup time	t_{HS}	30		ns
$\overline{HOLD}$ Hold time	t_{HH}	30		ns
$\overline{HOLD}$ High to Low-Z Output	t_{HLZ}		50	ns
$\overline{HOLD}$ Low to High-Z Output	t_{HHZ}		100	ns
Write cycle time	t_{WC}		5	ms
SCK to Low-Z output	t_{CLZ}	0		ns

Package Dimensions

unit : mm

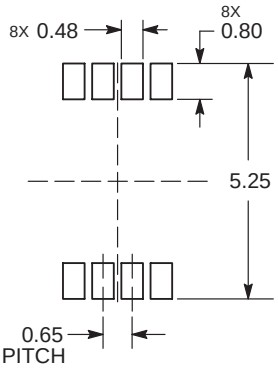
Micro8™
CASE 846A-02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

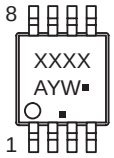
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

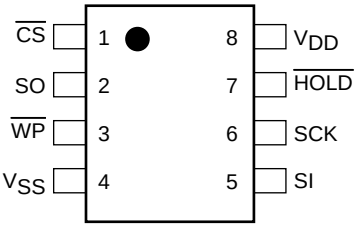
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

Pin Assignment



Pin Descriptions

PIN1	$\overline{CS}$	Chip select
PIN2	SO	Serial data output
PIN3	$\overline{WP}$	Write-protect
PIN4	V_{SS}	Ground
PIN5	SI	Serial data input
PIN6	SCK	Serial clock
PIN7	$\overline{HOLD}$	Hold
PIN8	V_{DD}	Power supply

Block Diagram

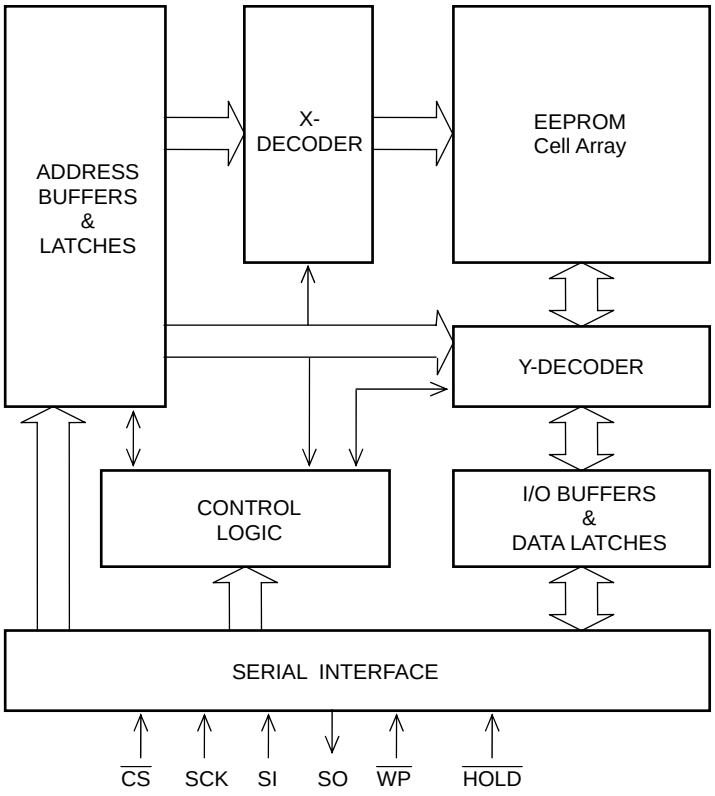


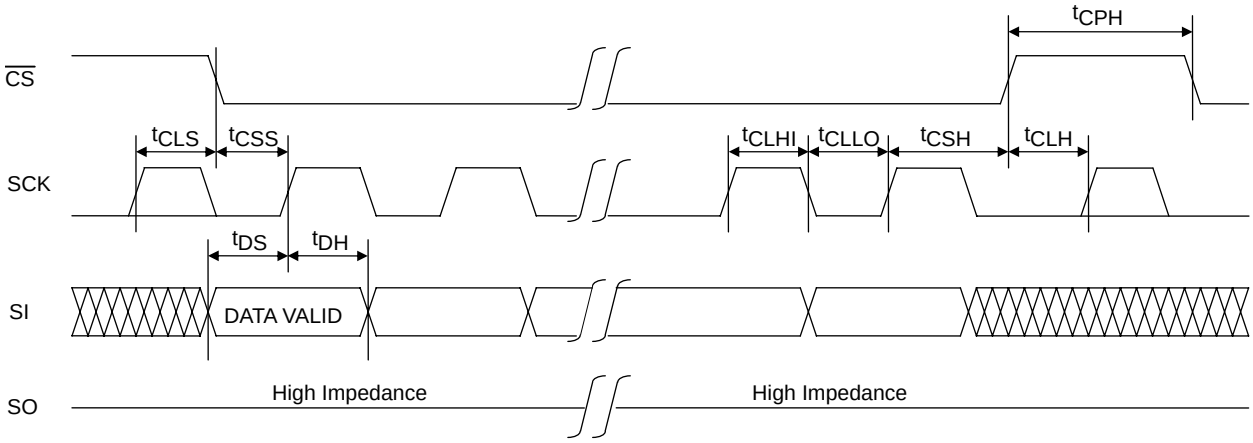
Table 1: Commands Summary

Command	The 1st bus cycle	The 2nd bus cycle	The 3rd bus cycle	The 4th bus cycle	The 5th bus cycle	The 6th bus cycle	The n-th bus cycle
Write enable (WREN)	06h						
Write disable (WRDI)	04h						
Status Register Read (RDSR)	05h						
Status Register Write (WRSR)	01h	DATA					
Read	03h	A15-A8	A7-A0				
Write	02h	A15-A8	A7-A0	PD *1	PD *1	PD *1	PD *1

Definition of Table 1 :
h = hexadecimal notation, A15 to A13 are don't care for all commands.
*1. PD: page write data. The arbitrary numbers of data of 1 to 32 bytes of byte unit for input.

Figure 2: Serial Input Timing Diagram

(SPI Mode 0)



(SPI Mode 3)

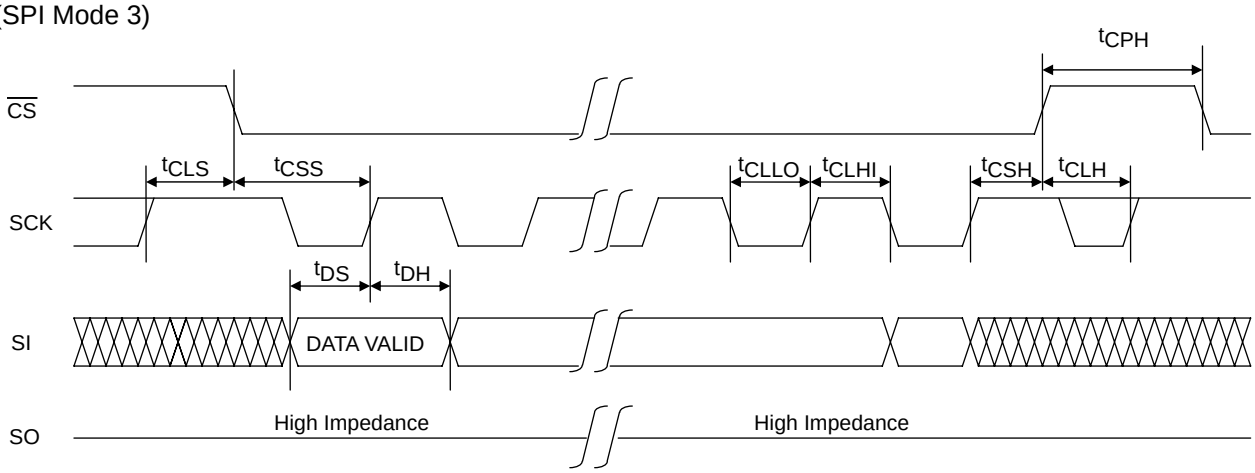
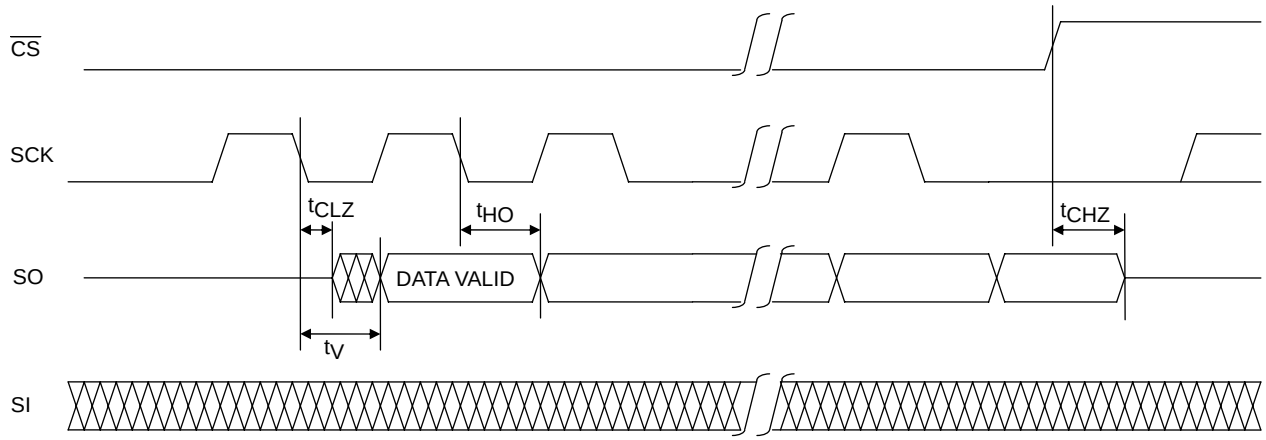
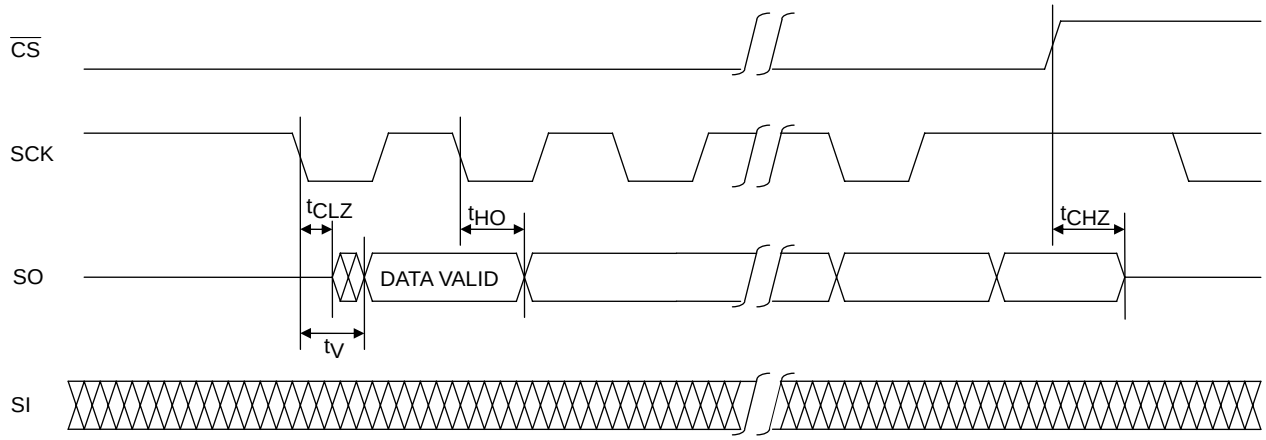


Figure 3: Serial Output Timing Diagram

(SPI Mode 0)



(SPI Mode 3)



Command definition

Table1 contains a command list and a brief summary of the commands. The following is a detailed description of the options initiated by each command.

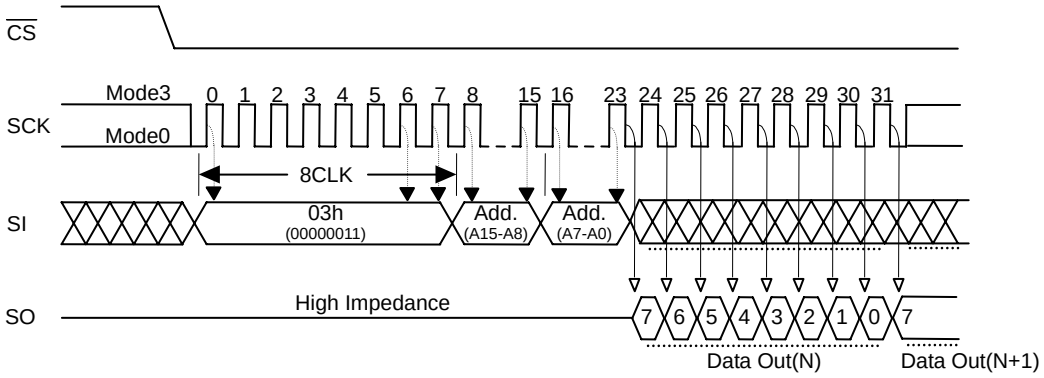
1. Read (Read)

The read operation is constituted from the 1st bus cycle to the 4th bus cycle. If 16-bit address is inputted after OP-code (03h), the data of the specified address will be outputted synchronizing with SCK. A data is outputted from the falling edge clock of the 4th bus cycle Bit0. Figure4 shows timing waveform of a Read operation.

While having inputted SCK, the increment of the address is automatically carried out inside a device, and data is outputted in order until the top address up to. If the data is outputted and the input of SCK continues still more, it returns to the lowest address (0000h) and a data output is continued.

By making $\overline{CS}$ into a logic high level, a device is deselecting, and read cycle is ended. Output terminal will be in a high impedance state.

Figure 4: Read Timing Diagram



■ A15 to A13: Don't Care
■ SI inputs the command and Address synchronizing with rising edge of 0 to 23rd SCK clock.
■ SO outputs the data synchronizing with falling edge of SCK of after 23rd SCK clock.

2. Status Register

The Status Register can perform detection state of a device and setup of protection. The register consists of 8 bits. The Status Register's contents are shown in Table2.

Table 2 : Status Register

Bit	Name	Logic	Function	Default at Power up
Bit0	$\overline{RDY}$	0	Ready state	0
		1	Busy state (Write operation progress)	
Bit1	WEN	0	Write prohibition state	0
		1	Write possible state	
Bit2	BP0	0	The block protect information Reference Status Registers BP0 and BP1	Non-volatile information
		1		
Bit3	BP1	0		Non-volatile Information
		1		
Bit4	X	0	Reserve Bit	0
Bit5	X	0	Reserve Bit	0
Bit6	X	0	Reserve Bit	0
Bit7	SRWP	0	Status Register Write enable state	Non-volatile Information
		1	Status Register Write disable state	

2-1. Status Register Read (RDSR)

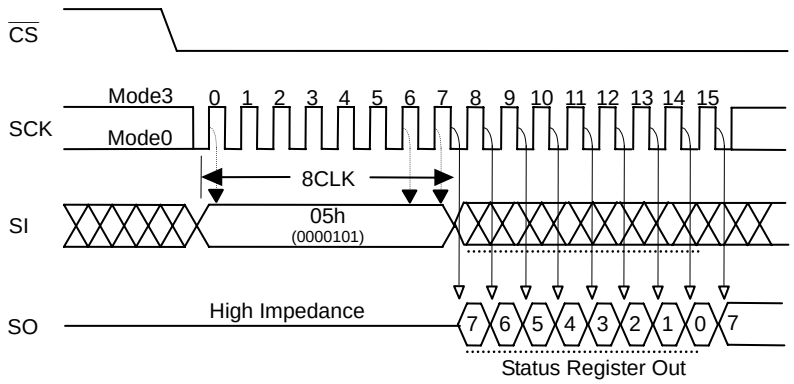
Status Register Read can read the Status Register's contents, moreover it can read also during the write operation. Figure5 shows timing waveform of a Status Register Read.

Status Register command consists of only the 1st bus, If OP-code (05h) dose writes in, synchronizing with falling edge of SCK, the Status Register's contents will be outputted from SRWP (Bit7).

If the data is outputted until $\overline{RDY}$ (Bit0), and also SCK input continues still more, it returns to SRWP and data output is continued. Data is outputted from the falling edge clock of the 1st bus cycle Bit0.

Status Register Read can be read always (also in case of inside of write cycle).

Figure 5: Read Status Register Timing Diagram



2-2. Status Register Write (WRSR)

By Status Register Write, BP0, BP1 and SRWP can be rewritten. $\overline{RDY}$, WEN, Bit4, Bit5 and Bit6 are read-only, BP0, BP1 and SRWP are non-volatile.

A timing waveform is shown in Figure6 and a flow chart is shown in Figure11.

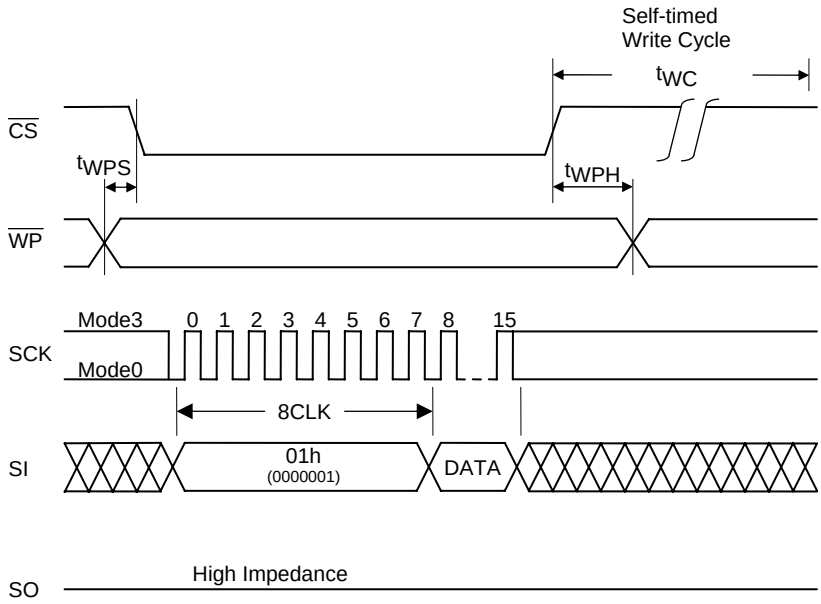
Status Register Write command consists of the 1st bus cycle and the 2nd bus cycle, and internal Write operation starts with the rising edge of $\overline{CS}$ after inputting data after OP-code (01h). Internal write operation is automatically performed inside the device and a Status Register Write rewrites BP0, BP1 and SRWP non-volatilized data. The write-in data to read-only bits ($\overline{RDY}$, WEN, Bit4, Bit5, Bit 6) are don't care.

The end of a Status Register Write is detectable with $\overline{RDY}$ of a Status Register Read.

The number of times of rewriting of a Status Register Write is 1,000 times (Min).

In order to perform a Status Register Write, it is necessary to change WEN of a Status Register into "1" state for $\overline{WP}$ pin.

Figure 6: Status Register Write Timing Diagram



2-3. Status Register Description

$\overline{RDY}$ (Bit0)

The end of a Write is detectable with $\overline{RDY}$. If device is in a busy state $\overline{RDY}$ is in "1", and the Write will be ended in "0" states.

WEN (Bit1)

It is detectable whether a Write is possible with WEN. If WEN is in "0" state, even if it inputs a Write command, Device will not perform write operation. If WEN is in "1" state, Write is possible to the area by which block protection is not carried out.

WEN is controllable with a Write Enable command and a Write disable command. WEN will be in "1" state with a Write Enable command (06h), and will be in "0" states with a Write disable command (04h).

Moreover, in the following state, automatically, WEN will be in "0" states and an unprepared Write will be prevented.

- At the time of a power-up
- After a write is completed
- After a Status Register Write is completed

* WEN keeps previous status, if input command is incomplete, execute write operation for protected address and not execute internal write.

BP0, BP1 (Bit2, 3)

Block protection BP0 and BP1 can set up the memory address area to be protected. Refer to Table 3 for setting conditions.

Table 3: Protection level setting conditions

Protection level (Level)	Status Register bit		Protection area
	BP1	BP0	
all area unprotect ion (0)	0	0	nothing
Upper 1/4 protection (1)	0	1	1800h to 1FFFh
Upper 1/2 protection (2)	1	0	1000h to 1FFFh
all area protection (3)	1	1	0000h to 1FFFh

SRWP (Bit7)

Status Register Write protection SRWP protects Status Register. When "1" state and $\overline{WP}$ pin are logic low levels, as for a Status Register Write command, they are disregarded, and as for BP0, BP1 and of a Status Register, and SRWP is protected. When $\overline{WP}$ pin is a logic high level, a Status Register is not protected irrespective of the state of SRWP. SRWP setting conditions are shown in Table 4.

Table 4: SRWP setting conditions

$\overline{WP}$ pin	SRWP	Mode	Status Register protection state	Protected Area	Unprotected Area
1	0	Software Protect (SPM)	Unprotect	Protect	Unprotect
0	0				
1	1				
0	1	Hardware Protect (HPM)	Protect	Protect	Unprotect

Bit4, Bit5, Bit6 are reserve bit.

3. Write Enable

Write Enable sets a Status Register WEN to "1" state. In order to perform the following operation, it is necessary to execute a Write Enable command first. A timing waveform is shown in Figure7. Write Enable command consists of only the 1st bus cycle, OP-code is 06h.

- Write
- Status Register Write

4. Write disable

Write disable sets a Status Register WEN to "0" states, and forbids an unprepared Write.
Figure8 shows timing waveform. Write Enable command consists of only the 1st bus cycle. OP-code is 04h.
To release from a Write disable state (WEN "0"), it should be performed the Write Enable command (06h).

Figure 7: Write Enable Timing Diagram

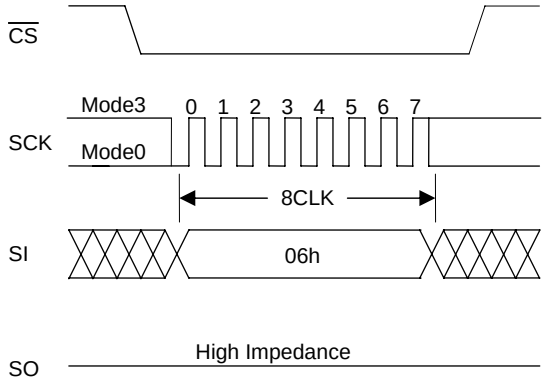
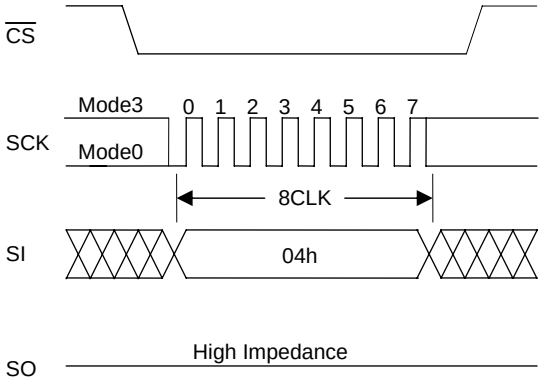


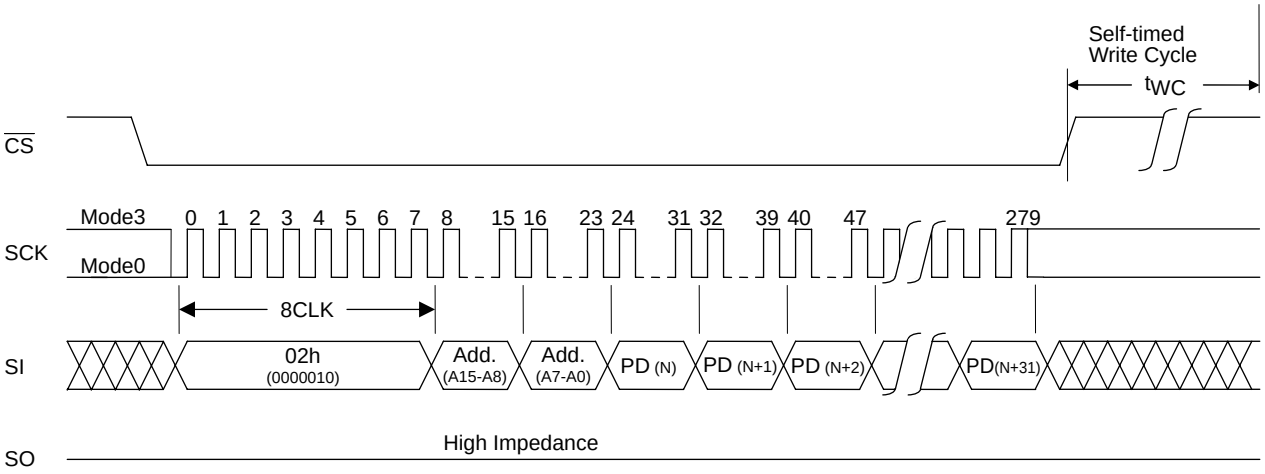
Figure 8: Write Disable Timing Diagram



5. Write

Page Write can write the arbitrary numbers of bytes of 1 to 32 bytes.
Figure9 shows timing waveform and a flow chart is shown in Figure12.
16-bit address is inputted after OP-code (02H). Then, loading is possible for write data during $\overline{CS}$ is low. When the data loaded exceeds 32 bytes, 32 bytes loaded at the end are written.
It is necessary to load write data per byte, and when it writes by loading the data below a byte unit, a normal write is not performed. Write cycle time fixed 5ms (Max) when execute 32 bytes page write.

Figure 9: Write

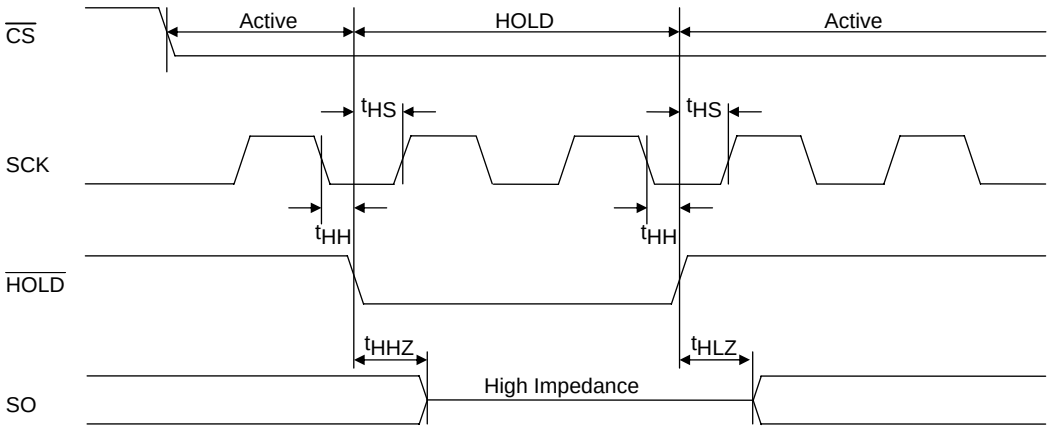


■ A15 to A13: Don't Care

6. Hold Function

$\overline{HOLD}$ pin is used in order to pause serial communication (hold state).
The timing waveform is shown in Figure10.
If $\overline{HOLD}$ starts to falling edge in the timing SCK on a logic low level, device will be in a hold state. And if $\overline{HOLD}$ starts to rising edge, Device will release from hold state in same timing.
Changes of $\overline{HOLD}$ are forbidden when CLK is High level.
If it is effective when $\overline{CS}$ is a logic low level, and when $\overline{CS}$ is rising edged, it will release from a hold state and serial communication will be reset.
In a hold state, SO is Hi-Z, SI and SCK is Don't Care.

Figure 10: Hold Command Timing Diagram



7. Hardware data protection

In order to prevent the unprepared writing at power-up, this device has the power-on reset function inside.

8. Software data protection

To prevent unprepared operation, this device ignores the command below conditions.

- There is no the timing of rising edge of $\overline{CS}$ during bus cycle when write command input.
- No byte unit of write data
- More than 2 bus cycles of the Status Resistor Write command input.

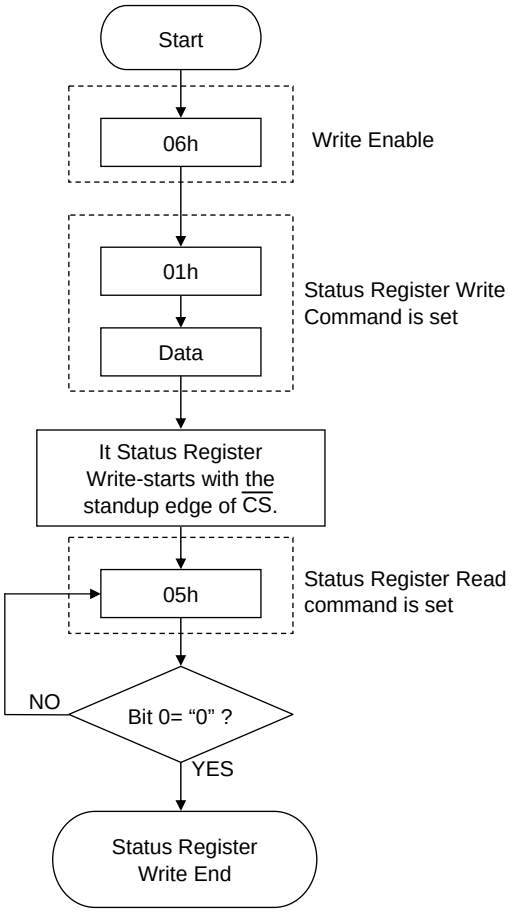
9. Power-up

Please make $\overline{CS}$ to high to prevent a careless writing when you turn on the power supply.
Please begin the command input of the read operation after 100µs (tPU_READ) from the state to which the power-supply voltage is 2.7V or more steady.
Please begin the command input of the write operation after 10ms (tPU_WRITE) from the state to which the power-supply voltage is 2.7V or more steady.

10. Decoupling capacitor

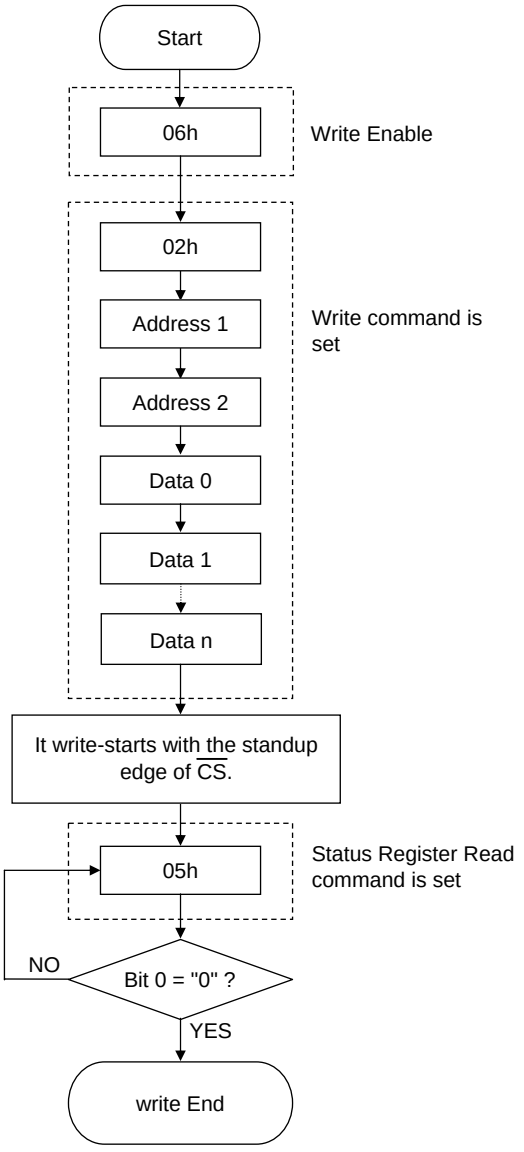
Ceramic capacitors (0.1µF) must be added between V_{DD} and V_{SS} to each device to assure stable EEPROM operation.

Figure 11: Status Register Write Flow Chart



It becomes a Write Disable automatically after Status Register Write.

Figure12: Write Flow Chart



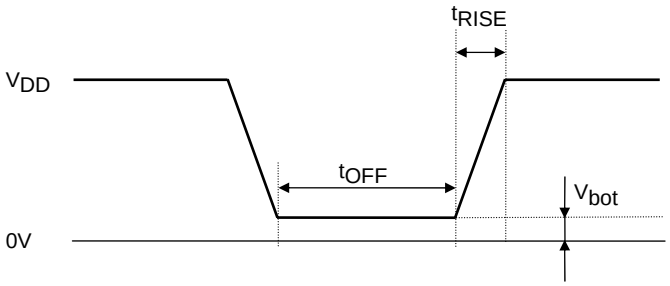
It becomes Write Disable automatically after write.

■ Application Notes

1) Precautions when turning on the power

This product contains a power-on reset circuit for preventing the inadvertent writing of data when the power is turned on. The following conditions must be met in order to ensure stable operation of this circuit. No data guarantees are given in the event of an instantaneous power failure during the internal write operation.

Parameter	symbol	V_{DD} = 2.7 to 5.5V			Unit
		min	typ	max	
Power rise time	t_{RISE}	–	–	100	ms
Power off time	t_{OFF}	10	–	–	ms
Power bottom voltage	V_{bot}	–	–	0.2	V



Notes:
1) $\overline{CS}$ = H.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LE25CB643TT-BH	Micro8 (Pb-Free / Halogen Free)	4000 / Tape &Reel